

IN THE CLAIMS

1. (Currently Amended) An integrated circuit comprising:
 - a first switch, a second switch and a third switch;
 - a first conductor and a second conductor, each having different first and second spans, respectively, in along a first dimension, wherein said the first span has a is greater span than said the second span, each of the first conductor and the second conductor being neither an input nor an output of a program controlled cell, at least one conductor of the first conductor and the second conductor to selectively couple to two independently controlled switches comprising the first switch and second switch;
 - ~~at least one conductor of said the first conductor and said the second conductor is selectively coupled to two independently controlled first and second switches, wherein~~
 - a first program controlled logic cell to drive drives said the at least one conductor through at least said the first switch without requiring traversal of another conductor; and
 - a second program controlled logic cell to drive drives said the at least one conductor through at least said the second switch without requiring traversal of another conductor; and
 - wherein said the first span conductor is selectively coupled configured to drive said the second span conductor through a third switch without requiring traversal of another span conductor, wherein said and wherein the first conductor span and said the second conductor span are spanning at least one common program controlled logic cell in along the first dimension.

2. (Currently Amended) The integrated circuit as set forth in claim 1, wherein ~~said~~ the switches comprise program controlled passgates.
3. (Currently Amended) The integrated circuit as set forth in claim 1, wherein ~~said~~ the switches comprise program controlled drivers/receivers.
4. (Currently Amended) The integrated circuit as set forth in claim 1, wherein ~~said~~ the switches comprise program controlled passgates and program controlled drivers/receivers.
5. (Currently Amended) The integrated circuit as set forth in claim 1, wherein at least one of ~~said~~ the switches has a program controlled on state and off state.
6. (Currently Amended) The integrated circuit as set forth in claim 1, wherein ~~said~~ the integrated circuit is implemented using process technology incorporating memory devices.
7. (Currently Amended) The integrated circuit as set forth in claim 1, wherein ~~said~~ the integrated circuit is implemented using process technology incorporating non-volatile memory devices.
8. (Currently Amended) The integrated circuit as set forth in claim 1, wherein ~~said~~ the integrated circuit is implemented using process technology incorporating fuse devices.

9. (Currently Amended) The integrated circuit as set forth in claim 1, wherein ~~said~~ the integrated circuit is implemented using process technology incorporating anti-fuse devices.

10. (Currently Amended) The integrated circuit as set forth in claim 1, wherein ~~said~~ the integrated circuit is implemented using process technology incorporating ferro-electric devices.

11. (Currently Amended) The integrated circuit as set forth in claim 1, further ~~comprises~~ comprising a third conductor having a third span, the third conductor being neither an input nor an output of a program controlled cell.

12. (Currently Amended) The integrated circuit as set forth in claim 11, wherein ~~said~~ the third ~~span~~ conductor to selectively couple[[s]] to ~~said~~ the first ~~span~~ conductor through a fourth switch without requiring traversal of another ~~span~~ conductor.

13. (Currently Amended) The integrated circuit as set forth in claim 12, wherein ~~said~~ the second span is equal to ~~said~~ the third span and ~~said~~ the third span is ~~in~~ along the first dimension.

14. (Currently Amended) The integrated circuit as set forth in claim 13, wherein ~~said~~ the second conductor spans ~~span is spanning~~ at least one different program controlled logic cell than ~~said~~ the third conductor ~~span in~~ along the first dimension.

15. (Currently Amended) The integrated circuit as set forth in claim 11, wherein ~~said~~ the third span is in along a second dimension.

16. (Currently Amended) The integrated circuit as set forth in claim 15, wherein ~~said~~ the third span conductor is configured to selectively couples couple to at least one ~~span~~ conductor of ~~said~~ the first span conductor and ~~said~~ the second span conductor through a fifth switch without requiring traversal of another ~~span~~ conductor.

17. (Currently Amended) The integrated circuit as set forth in claim 16, wherein ~~said~~ the third conductor span is equal in span to ~~said~~ the at least one span conductor of the first conductor and the second conductor.

18. (Currently Amended) The integrated circuit as set forth in claim 11, wherein ~~said~~ the first conductor span, said the second conductor span and said the third conductor span are have three different spans ~~in along~~ the first dimension.

19. (Currently Amended) The integrated circuit as set forth in claim 18, wherein ~~said~~ the second span conductor is configured to selectively couples couple to ~~said~~ the third conductor span through a sixth switch without requiring traversal of another conductor span.

20. (Currently Amended) The integrated circuit as set forth in claim 18, further comprises at least three conductors having three different spans ~~in along~~ a second dimension comprising:

a fourth conductor having a fourth span along a second dimension;

a fifth conductor having a fifth span along the second dimension; and
a sixth conductor having a sixth span along the second dimension, the fourth,
fifth and sixth spans being different than each other, and wherein each of the fourth, fifth
and sixth conductors are neither an input nor an output of a program controlled cell.

21. (Currently Amended) The integrated circuit as set forth in claim 20, wherein at least one ~~span of said the fourth, fifth and sixth conductors~~ three different spans in along the second dimension is configured to selectively ~~couples~~ couple to at least one ~~span of said the first, second and third spans~~ conductors through a seventh switch without requiring traversal of another ~~span~~ conductor.

22. (Currently Amended) The integrated circuit as set forth in claim 19, further comprising a fourth conductor having a fourth span, wherein ~~said the fourth span conductor to~~ selectively ~~couples~~ couple to at least one ~~span conductor of said the first span conductor, said the second span conductor and said the third span conductor~~ through a ~~seventh~~ an eighth switch without requiring traversal of another span and the fourth conductor being neither an input nor an output of a program controlled cell.

23. (Currently Amended) The integrated circuit as set forth in claim 22, wherein ~~said the fourth span is in along~~ one of a dimension of a group consisting of ~~said the first dimension and said the second dimension.~~

24. (Currently Amended) A method ~~of providing an integrated circuit~~ comprising: providing a first conductor and a second conductor, each having different first and second spans, respectively, ~~in along~~ a first dimension, wherein ~~said the~~

first span ~~has a~~ is greater span than ~~said the~~ second span, each conductor of the first conductor and the second conductor being neither an input nor an output of a program controlled cell;

selectively coupling at least one conductor of ~~said the~~ first conductor and ~~said the~~ second conductor to two independently controlled switches comprising a first switch and a second switch ~~switches, wherein a first program controlled logic cell drives said~~

driving the at least one conductor through ~~at least said the~~ first switch without requiring traversal of another conductor, using a first program controlled cell; and a second program controlled logic cell drives said

driving the at least one conductor through ~~at least said the~~ second switch without requiring traversal of another conductor using a second program controlled cell; and

selectively coupling ~~said the~~ first ~~span~~ conductor to drive ~~said the~~ second ~~span~~ conductor through a third switch without requiring traversal of another ~~span~~ conductor, wherein ~~said the~~ first ~~conductor~~ span and ~~said the~~ second ~~conductor~~ span are spanning at least one common program controlled logic cell ~~in~~ along the first dimension.

25. (Currently Amended) The method as set forth in claim 24, further ~~comprises~~ comprising providing a third conductor having a third span, the third conductor being neither an input nor an output of a program controlled cell.

26. (Currently Amended) The method as set forth in claim 25, further comprising: providing a fourth switch; and ~~wherein said~~

selectively coupling the third span conductor selectively couples to said the
first span conductor through the [[a]] fourth switch without requiring traversal of another
span conductor.

27. (Currently Amended) The method as set forth in claim 26, wherein the second
span is equal to said the third span and said wherein the third span is in along the first
dimension.

28. (Currently Amended) The method as set forth in claim 27, wherein the second
conductor span spans at least one different program controlled logic cell than said the
third conductor span in along the first dimension.

29. (Currently Amended) The method as set forth in claim 25, wherein said the third
span is in along a second dimension.

30. (Currently Amended) The method as set forth in claim 29, further comprising:
providing a fifth switch; and
selectively coupling said the third span conductor to at least one span
conductor of said the first span conductor and said the second span conductor through the
[[a]] fifth switch without requiring traversal of another span conductor.

31. (Currently Amended) The method as set forth in claim 30, wherein said the third
conductor span is equal in span to said the at least one span conductor of the first
conductor and the second conductor.

32. (Currently Amended) The method as set forth in claim 25, wherein ~~said~~ the first span, ~~said~~ the second span and ~~said~~ the third span are three different spans ~~in~~ along ~~said~~ the first dimension.

33. (Currently Amended) The method as set forth in claim 32, further comprising:
providing a sixth switch; and
selectively coupling ~~said~~ the second span conductor to ~~said~~ the third span conductor through the ~~the~~ [[a]] sixth switch without requiring traversal of another ~~span~~ conductor.

34. (Currently Amended) The method as set forth in claim 32, further comprising:
~~providing at least three different conductors having three different spans in a second dimension~~
a fourth conductor having a fourth span along a second dimension;
a fifth conductor having a fifth span along the second dimension; and
a sixth conductor having a sixth span along the second dimension, the fourth, fifth and sixth spans being different than each other, and wherein each of the fourth, fifth and sixth conductors are neither an input nor an output of a program controlled cell.

35. (Currently Amended) The method as set forth in claim 34, further comprising
providing a seventh switch, wherein at least one span of ~~said~~ the fourth, fifth and sixth ~~three different span conductors in the second dimension~~ to selectively couples ~~couple~~ couple to at least one span of ~~said~~ the first, second and third spans conductors through ~~the~~ [[a]] the seventh switch without requiring traversal of another ~~span~~ conductor.

36. (Currently Amended) The method as set forth in claim 33, further comprising providing a fourth conductor having a fourth span, wherein ~~said~~ the fourth span conductor to selectively couple[[s]] to at least one span conductor of ~~said~~ the first span conductor, ~~said~~ the second span conductor and ~~said~~ the third span conductor through [[a]]-~~seventh~~ an eighth switch without requiring traversal of another span conductor and the fourth conductor being neither an input nor an output of a program controlled cell.

37. (Currently Amended) The method as set forth in claim 36, wherein ~~said~~ the fourth span is ~~in~~ along one of a dimension of a group consisting of ~~said~~ the first dimension and ~~said~~ the second dimension.

38. (Currently Amended) An integrated circuit comprising:
a first conductor and a second conductor, each having a different first and second spans, respectively, ~~in~~ along a first dimension, wherein ~~said~~ the first conductor span and ~~said~~ the second conductor span are spanning at least one common program controlled logic cell ~~in~~ along the first dimension;
a third conductor having a third span ~~in~~ along a second dimension, each of the first conductor, the second conductor and the third conductor being neither an input nor an output of a program controlled cell; said
a first switch and second switch, the first span conductor to selectively couples couple to ~~said~~ the third span conductor through [[a]] the first switch without requiring traversal of another span conductor, and ~~said~~ the second span conductor to selectively couple[[s]] to ~~said~~ the first span conductor through [[a]] the second switch without requiring traversal of ~~any other span another conductor~~; and

a third switch and a fourth switch, at least one conductor of ~~said~~ the first conductor, ~~said~~ the second conductor and ~~said~~ the third conductor to selectively couple ~~couples~~ to two independently controlled switches comprising the third and fourth switches; ~~wherein~~
a first program controlled ~~logic~~ cell to drive ~~drives~~ ~~said~~ the at least one conductor through ~~at least~~ ~~said~~ the third switch without requiring traversal of another conductor; and
a second program controlled ~~logic~~ cell to drive ~~drives~~ ~~said~~ the at least one conductor through ~~at least~~ ~~said~~ the fourth switch without requiring traversal of another conductor.

39. (Currently Amended) The integrated circuit as set forth in claim 38, wherein ~~said~~ the first span is greater than ~~said~~ the second span.

40. (Currently Amended) The integrated circuit as set forth in claim 38, wherein ~~said~~ the second span is greater than ~~said~~ the first span.

41. (Currently Amended) The integrated circuit as set forth in claim 40, further comprising a fourth conductor having a fourth span ~~in~~ along the first dimension, wherein ~~said~~ the fourth span is greater than ~~said~~ the second span and the fourth conductor being neither an input nor an output of a program controlled cell.

42. (Currently Amended) The integrated circuit as set forth in claim 41 ~~38~~, wherein ~~said~~ the switches comprise program controlled passgates.

43. (Currently Amended) The integrated circuit as set forth in claim 41 38, wherein ~~said~~ the switches comprise program controlled drivers/receivers.

44. (Currently Amended) The integrated circuit as set forth in claim 41 38, wherein ~~said~~ the switches comprise program controlled passgates and program controlled drivers/receivers.

45. (Currently Amended) The integrated circuit as set forth in claim 41 38, wherein at least one of ~~said~~ the switches has a program controlled on state and off state.

46. (Currently Amended) The integrated circuit as set forth in claim 41 38, wherein ~~said~~ the integrated circuit is implemented using process technology incorporating memory devices.

47. (Currently Amended) The integrated circuit as set forth in claim 41 38, wherein ~~said~~ the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

48. (Currently Amended) The integrated circuit as set forth in claim 41 38, wherein ~~said~~ the integrated circuit is implemented using process technology incorporating fuse devices.

49. (Currently Amended) The integrated circuit as set forth in claim 41 38, wherein ~~said~~ the integrated circuit is implemented using process technology incorporating anti-fuse devices.

50. (Currently Amended) The integrated circuit as set forth in claim 41 ~~38~~, wherein ~~said the~~ integrated circuit is implemented using process technology incorporating ferro-electric devices.

51. (Currently Amended) The integrated circuit as set forth in claim 41, further comprising a fifth switch, wherein said the fourth span conductor to selectively couple[[s]] said to the second span conductor through [[a]] the fifth switch without requiring traversal of another conductor.

52. (Currently Amended) A method ~~of providing an integrated circuit~~ comprising:
providing a first conductor and a second conductor, each having a different first and second spans, respectively, ~~in the~~ along a first dimension, wherein ~~said~~ each of the first conductor span and said the second conductor span are spanning at least one common program controlled logic cell along the first dimension;
providing a third conductor having a third span ~~in~~ along a second dimension, each conductor of the first conductor, the second conductor and the third conductor being neither an input nor an output of a program controlled cell;
selectively coupling ~~said the~~ first span conductor to ~~said the~~ second span conductor through a first switch without requiring traversal of another span conductor;

selectively coupling ~~said the~~ first span conductor to ~~said the~~ second span conductor through a second switch without requiring traversal of ~~any other span another conductor~~; and

selectively coupling at least one conductor of ~~said the~~ first conductor, ~~said the~~ second conductor and ~~said the~~ third conductor to two independently controlled third and fourth switches; ~~wherein a first program controlled logic cell drives said~~

driving the at least one conductor, using a first program controlled cell, through at least ~~said the~~ third switch without requiring traversal of another conductor; and

driving the ~~a second program controlled logic cell drives said~~ at least one conductor, using a second program controlled cell, through at least ~~said the~~ fourth switch without requiring traversal of another conductor.

53. (Currently Amended) The method as set forth in claim 52, wherein ~~said the~~ first span is greater than ~~said the~~ second span.

54. (Currently Amended) The method as set forth in claim 52, wherein ~~said the~~ second span is greater than ~~said the~~ first span.

55. (Currently Amended) The method as set forth in claim 54, further comprising providing a fourth conductor having a fourth span ~~in~~ along said the first dimension, wherein ~~said the~~ fourth span is greater than ~~said second span~~ and the fourth conductor is neither an input nor an output of a program controlled cell.

56. (Currently Amended) The method as set forth in claim 55, further comprising selectively coupling-said the fourth span conductor to said the second span conductor through a fifth switch without requiring traversal of another conductor.

57. (New) An integrated circuit comprising:

a first switch;

a first conductor, a second conductor and a third conductor, each having a respectively different first span, second span and third span along a first dimension, wherein the first span is greater than the second span, wherein the first span is greater than the third span, and wherein each of the first conductor, the second conductor and the third conductor spans at least one common program controlled cell along the first dimension;

a fourth conductor, a fifth conductor and a sixth conductor, each having a respectively different fourth span, fifth span and sixth span along a second dimension, wherein the fourth span is greater than the fifth span, wherein the fourth span is greater than the sixth span, and wherein each of the fourth conductor, the fifth conductor and the sixth conductor spans at least one common program controlled cell along the second dimension, the first conductor to selectively couple to the fourth conductor through the first switch without requiring traversal of another conductor; and

wherein each conductor of the first conductor, the second conductor, the third conductor, the fourth conductor, the fifth conductor and the sixth conductor is neither an input nor an output of a program controlled cell.

58. (New) The integrated circuit as set forth in claim 57, further comprising a second switch, wherein the second conductor is configured to selectively couple to the fifth conductor through the second switch without requiring traversal of another conductor.

59. (New) The integrated circuit as set forth in claim 57, wherein the first switch comprises program controlled passgates.

60. (New) The integrated circuit as set forth in claim 57, wherein the first switch comprises program controlled drivers/receivers.

61. (New) The integrated circuit as set forth in claim 57, wherein the first switch comprises program controlled passgates and program controlled drivers/receivers.

62. (New) The integrated circuit as set forth in claim 57, wherein the first switch has a program controlled on state and off state.

63. (New) The integrated circuit as set forth in claim 57, wherein the integrated circuit is implemented using process technology incorporating memory devices.

64. (New) The integrated circuit as set forth in claim 57, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

65. (New) The integrated circuit as set forth in claim 57, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

66. (New) The integrated circuit as set forth in claim 57, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

67. (New) A method comprising:

providing a first conductor, a second conductor and a third conductor, each having a respective different first span, second span and third span along a first dimension, wherein the first span is greater than the second span, wherein the first span is greater than the third span, and wherein each of the first conductor, the second conductor and the third conductor span at least one common program controlled cell along the first dimension;

providing a fourth conductor, a fifth conductor and a sixth conductor having a respective different fourth span, fifth span and sixth span along a second dimension, wherein the fourth span is greater than the fifth span, wherein the fourth span is greater than the sixth span, and wherein each of the fourth conductor, the fifth conductor and the sixth conductor span at least one common program controlled cell along the second dimension, each conductor of the first conductor, the second conductor, the third conductor, the fourth conductor, the fifth conductor and the sixth conductor being neither an input nor an output of a program controlled cell; and selectively coupling the first conductor to the fourth conductor through a first switch without requiring traversal of another conductor.

68. (New) The method as set forth in claim 67, further comprising selectively coupling the second conductor to the fifth conductor through a second switch without requiring traversal of another conductor.

69. (New) An integrated circuit having a span, comprising:

a first switch;

a first conductor, a second conductor and a third conductor, each having a respective different first span, second span and third span along a first dimension, wherein the first span is greater than at least one of the second span and the third span, wherein each of the first span, the second span and the third span is less than the span of the integrated circuit along the first dimension, and wherein the first conductor, the second conductor and the third conductor are spanning at least one common program controlled cell along the first dimension;

a fourth conductor and a fifth conductor having a respective different fourth span and fifth span along a second dimension, wherein the fourth span is greater than the fifth span, wherein the fourth span is less than the span of the integrated circuit along the second dimension, and wherein the fourth conductor and the fifth conductor are spanning at least one common program controlled cell along the second dimension, the first conductor to selectively couple to the fourth conductor through the first switch without requiring traversal of another conductor; and

wherein each conductor of the first conductor, the second conductor, the third conductor, the fourth conductor and the fifth conductor is neither an input nor an output of a program controlled cell.

70. (New) The integrated circuit as set forth in claim 69, further comprising a second switch, wherein the second conductor is configured to selectively couple to the fifth conductor through the second switch without requiring traversal of another conductor.

71. (New) The integrated circuit as set forth in claim 69, wherein the integrated circuit consists of a core.

72. (New) The integrated circuit as set forth in claim 69, wherein the integrated circuit consists of a core and I/O to core interfaces.

73. (New) The integrated circuit as set forth in claim 69, wherein the integrated circuit excludes I/O logic blocks.

74. (New) The integrated circuit as set forth in claim 69, wherein the integrated circuit excludes I/O logic blocks and I/O to core interfaces.

75. (New) The integrated circuit as set forth in claim 69, wherein the first switch comprises program controlled passgates.

76. (New) The integrated circuit as set forth in claim 69, wherein the first switch comprises program controlled drivers/receivers.

77. (New) The integrated circuit as set forth in claim 69, wherein the first switch comprises program controlled passgates and program controlled drivers/receivers.

78. (New) The integrated circuit as set forth in claim 69, wherein the first switch comprises has a program controlled on state and off state.

79. (New) The integrated circuit as set forth in claim 69, wherein the integrated circuit is implemented using process technology incorporating memory devices.

80. (New) The integrated circuit as set forth in claim 69, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

81. (New) The integrated circuit as set forth in claim 69, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

82. (New) The integrated circuit as set forth in claim 69, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

83. (New) A method comprising:
providing a first conductor, a second conductor and a third conductor, each having a respective different first span, second span and third span along a first dimension, wherein the first span is greater than either the second span or the third span, and wherein each of the first conductor, the second conductor and the third conductor are spanning at least one common program controlled cell along the first dimension;

providing a fourth conductor and a fifth conductor, each having a respectively different fourth span and fifth span along a second dimension, wherein the fourth span is greater than the fifth span, and wherein each of the fourth conductor and the fifth conductor are spanning at least one common program controlled cell along the second dimension;

each conductor of the first conductor, the second conductor, the third conductor, the fourth conductor and the fifth conductor being neither an input nor an output of a program controlled cell; and

selectively coupling the first conductor to the fourth conductor through a first switch without requiring traversal of another conductor.

84. (New) The method as set forth in claim 83, further comprising selectively coupling the second conductor to the fifth conductor through a second switch without requiring traversal of another conductor.

85. (New) The method as set forth in claim 83, wherein the integrated circuit consists of a core.

86. (New) The method as set forth in claim 83, wherein the integrated circuit consists of a core and I/O to core interfaces.

87. (New) The method as set forth in claim 83, wherein the integrated circuit excludes I/O logic blocks.

88. (New) The method as set forth in claim 83, wherein the integrated circuit excludes I/O logic blocks and I/O to core interfaces.